WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory array comprising a plurality of memory cells and a plurality of dummy cells;

a row decoder connected to the memory array;

a column selector that selects a normal column of the plurality of memory cells;

an amplifier circuit that amplifies data in the memory cell selected by the row decoder and the column selector;

a dummy control circuit that selectively activates, through a plurality of dummy word lines, at least one dummy cell among the plurality of dummy cells with respect to each of the dummy word lines;

a dummy column selector that selects a signal from the dummy cell activated by the dummy control circuit; and

an amplifier control circuit that generates an amplifier startup signal for the amplifier circuit, based on the signal selected by the dummy column selector.

2. The semiconductor memory device according to claim 1,

wherein the memory array comprises a plurality of dummy columns comprising the plurality of dummy cells and a plurality of dummy bit lines that are connected commonly to the plurality of dummy cells in the plurality of dummy columns, and

the plurality of dummy bit lines are connected to the dummy column selector.

3. The semiconductor memory device according to claim 2,

wherein the plurality of dummy word lines are connected to the memory array from a same side as a side where the amplifier circuit is placed, and are connected respectively to a part of the plurality of dummy cells included in the plurality of dummy columns.

4. The semiconductor memory device according to claim 2,

wherein the plurality of dummy word lines are connected to the memory array from a side opposite to a side where the amplifier circuit is placed, and are connected respectively to a part of the plurality of dummy

cells included in the plurality of dummy columns.

5. The semiconductor memory device according to claim 2, wherein the plurality of dummy cells connected to the dummy word lines are placed with respect to the memory array at an edge portion on an opposite side to a side where the amplifier circuit is placed.

6. The semiconductor memory device according to claim 1,

wherein the memory array comprises a dummy column and a plurality of dummy rows that include the plurality of dummy cells,

the plurality of dummy word lines are connected to the plurality of dummy rows, and

the dummy column comprises one dummy bit line.

7. The semiconductor memory device according to claim 1,

wherein the memory array comprises a dummy column including the plurality of dummy cells, and

the plurality of dummy word lines respectively are connected to the dummy cells placed at different positions on the dummy column.

8. The semiconductor memory device according to claim 6, wherein the dummy bit line is connected to the dummy column selector.

9. The semiconductor memory device according to claim 8,

wherein the column selector comprises a transfer gate, and

the dummy column selector comprises a transfer gate having a same configuration as that of the transfer gate included in the column selector.

10. The semiconductor memory device according to claim 9, wherein a transistor constituting the transfer gate that is connected to the dummy bit line and is included in the dummy column selector has a source and a drain that are short-circuited.

11. The semiconductor memory device according to claim 1, wherein the dummy control circuit comprises a memory circuit that stores a test result.

12. The semiconductor memory device according to claim 11, further

comprising a defect test terminal that is connected to the amplifier control circuit and measures a current of the dummy cells.

13. The semiconductor memory device according to claim 11, further comprising a defect test terminal that is connected to the amplifier control circuit and measures an output timing of the amplifier startup signal.

14. The semiconductor memory device according to claim 11, wherein the memory circuit is a nonvolatile memory circuit.

15. The semiconductor memory device according to claim 14, wherein the nonvolatile memory circuit comprises a fuse that can be disconnected with a laser.